REMARKS

Reconsideration of this application as amended is respectfully requested.

Claims 1-15 are pending. Claims 1-15 stand rejected.

Claims 1, 6, and 11 have been amended. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Rejections Under 35 U.S.C. § 103(a)

Claims 1-3, 5-8, 10-13, and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,480,948 of Virajpet et al. ("Virajpet") and U.S. Patent No. 6,262,594 of Cheung et al. ("Cheung").

It is respectfully submitted that Virajpet does not teach or suggest a combination with Cheung and that Cheung does not teach or suggest a combination with Virajpet. It would be impermissible hindsight based on applicants' own disclosure to incorporate the configurable memory map of Virajpet into the method for configuring groups of pads of a system on a chip of Cheung. Moreover, such a combination would still lack the limitation of "searching for a valid secondary initialization routine."

In rejecting claims 1-3, 5-8, 10-13, and 15 under 35 U.S.C. § 103(a) as being unpatentable over Virajpet and Cheung, the Examiner has stated that

> Regarding claims 1, 6, and 11, Virajpet et al. teaches a system for memory aliasing system. The processor is able to read from an internal ROM (31) for initialization (configuration) or boot code processing (col. 3, lines 1-16; col. 4, lines 5-23). Section (31) of the memory map is configurable, and during a first time period, the configurable section is aliased so that when the processor attempts to access this section (internal ROM), the access is directed toward the external ROM (20) under control of the bus/memory controller. Thus, when the processor seeks to address 00000000h, the access is directed toward an external non-volatile memory.
>
> The difference between the claimed subject matter and that of Virajpet et al., disclosed supra, is that the claims recite that the aliasing is done for a

> configurable system-on-chip system, as well as that the external memory is a flash memory. Cheung et al. teaches a configurable system-on-chip design. According to Figure 4, which illustrates specific modules that may be incorporated onto a system-on-chip configuration, Cheung et al. teaches an external flash ROM (non-volatile memory) with a flash ROM interface (col. 7, lines 56-60). Also, an erasable read-only-memory is taught for storing control values (col. 3, lines 14-16), where the ROM is found on the system-on-chip. Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Virajpet et al. and Cheung et al. before him at the time the invention was made to modify the aliasing system of Virajpet et al. to include the system-on-chip design of Cheung et al., because then a single integrated circuit chip would yield advantages of cost reduction, low power consumption, space savings and ruggedness, as taught by Cheung et al.

(Office Action mailed February 20, 2003, page 2, paragraphs 3-4)

Applicants respectfully submit that amended claim 1 is not rendered obvious by Virajpet in view of Cheung. Amended claim 1 includes the following limitations

> A method for multiple memory aliasing for a configurable system-on-a-chip, comprising:
>
> executing code from a read-only memory (ROM) internal memory, said ROM internal memory having an alias;
>
> searching for a valid secondary initialization routine;
>
> locating a configuration program in the ROM internal memory;
>
> disabling the ROM internal memory alias; and
>
> jumping to the secondary initialization routine located in a FLASH external memory.

(Amended Claim 1) (Emphasis added)

Applicants respectfully submit that Virajpet does not include this limitation, nor does the combination of Virajpet and Cheung. Furthermore, applicants respectfully contend that the Examiner has mistakenly equated the "system on a chip" disclosed by Cheung, which allows for the pads to be shared among function modules, with the "configurable system-on-a-chip" disclosed by the claimed present invention.

The system on a chip of Cheung does not claim to be configurable. Rather, the use of the pads is configurable, allowing a sharing of pads. In contrast, a configurable system-on-a-chip ("CSOC") integrates a CPU, an internal system bus, programmable logic, and various system resources all interconnected and communicating via the internal system bus on a single chip. Most CSOCs are comprised of core electronics (e.g., CPU, RAM, ROM, DMA, etc.) at their center and input/output electronics, or an IO ring, at their periphery. Figure 1 of the present application illustrates a CSOS.

For these reasons, applicants respectfully submit that amended claim 1 is not rendered obvious by Virajpet in view of Cheung. Given that claims 2-5 depend directly or indirectly from claim 1, applicants respectfully submit that claims 2-5 are likewise not rendered obvious by Virajpet in view of Cheung. Furthermore, given that independent claims 6 and 11 contain the same limitations as claim 1, and given that claims 7-10 and 12-15 depend directly or indirectly from claims 6 and 11, respectively, applicants respectfully submit that claims 6-15 are likewise not rendered obvious by Virajpet in view of Cheung.

Claims 4, 9, and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Virajpet, Cheung and U.S. Patent No. 6,401,164 of Bartoli et al. ("Bartoli").

It is also respectfully submitted that Virajpet and Cheung do not teach or suggest a combination with Bartoli and that Bartoli does not teach or suggest a combination with Virajpet and Cheung. It would be impermissible hindsight based on applicants' own disclosure to incorporate the configurable memory map of Virajpet and the method for configuring groups of pads of a system on a chip of Cheung into the memory device of Bartoli. Moreover, such a combination would still lack the limitations of amended claim 1 as discussed above.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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